FIG. 1

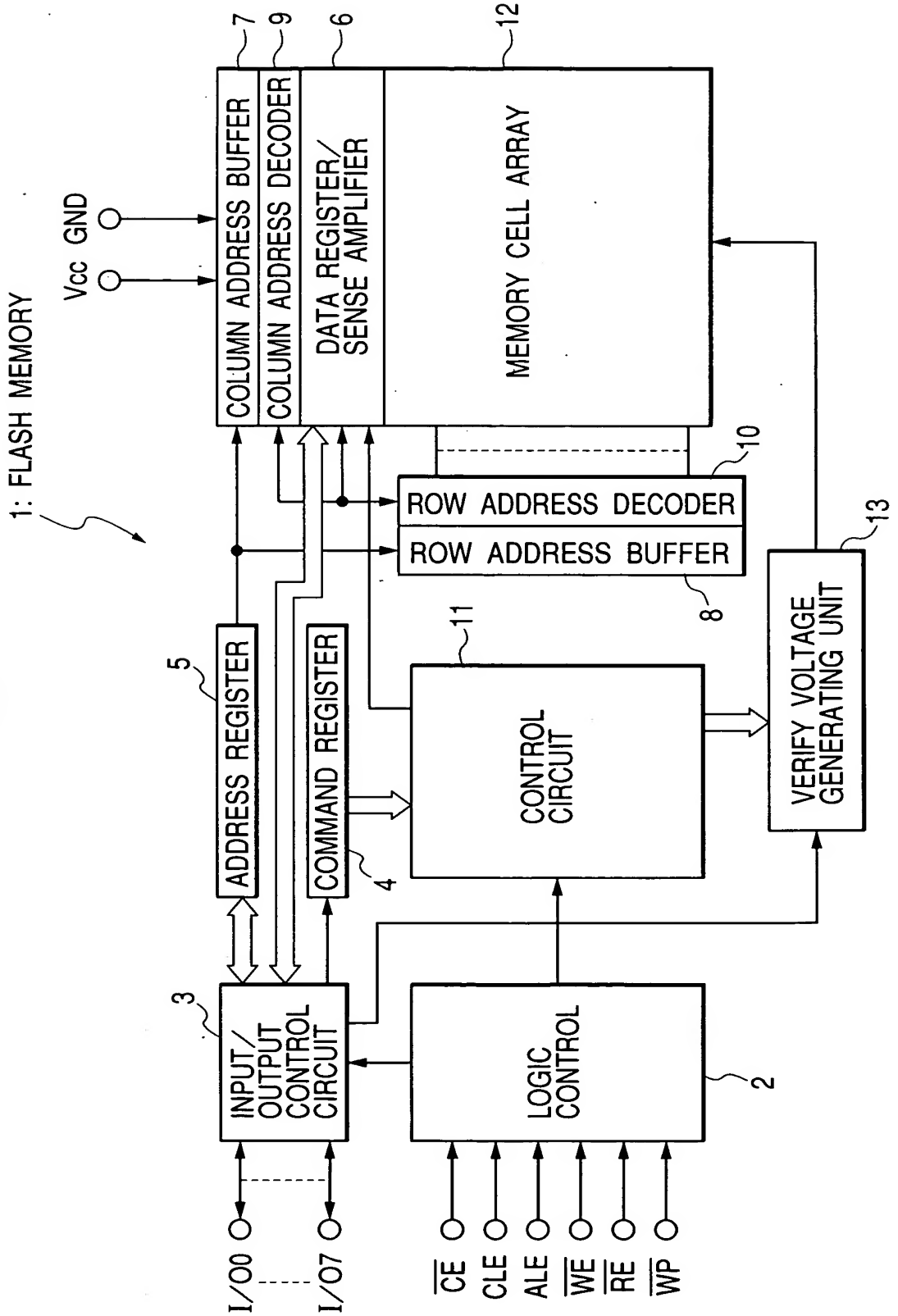

1: FLASH MEMORY
Vcc
GND
COLUMN ADDRESS BUFFER
COLUMN ADDRESS DECODER
DATA REGISTER/ SENSE AMPLIFIER
MEMORY CELL ARRAY
ROW ADDRESS DECODER
ROW ADDRESS BUFFER
ADDRESS REGISTER
COMMAND REGISTER
CONTROL CIRCUIT
VERIFY VOLTAGE GENERATING UNIT
INPUT/ OUTPUT CONTROL CIRCUIT
LOGIC CONTROL
I/O0
I/O7
CE
CLE
ALE
WE
RE
WP
7
9
6
12
10
13
8
11
5
4
3
2

FIG. 2

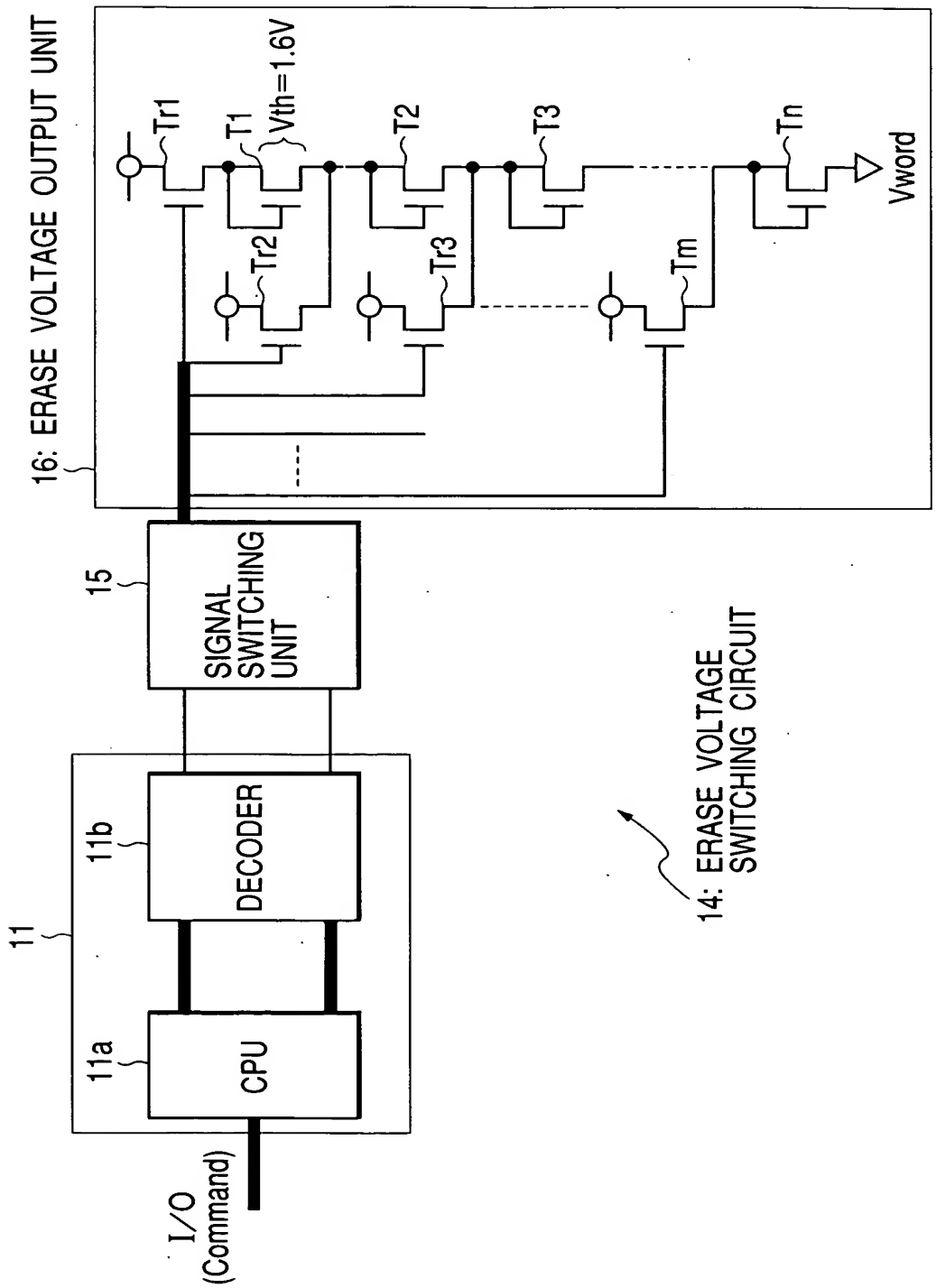

16: ERASE VOLTAGE OUTPUT UNIT
Tr1
T1
Vth=1.6V
T2
T3
Tn
Vword
Tr2
Tr3
Tm
15
SIGNAL SWITCHING UNIT
11
11b
DECODER
11a
CPU
I/O (Command)
14: ERASE VOLTAGE SWITCHING CIRCUIT

FIG. 3

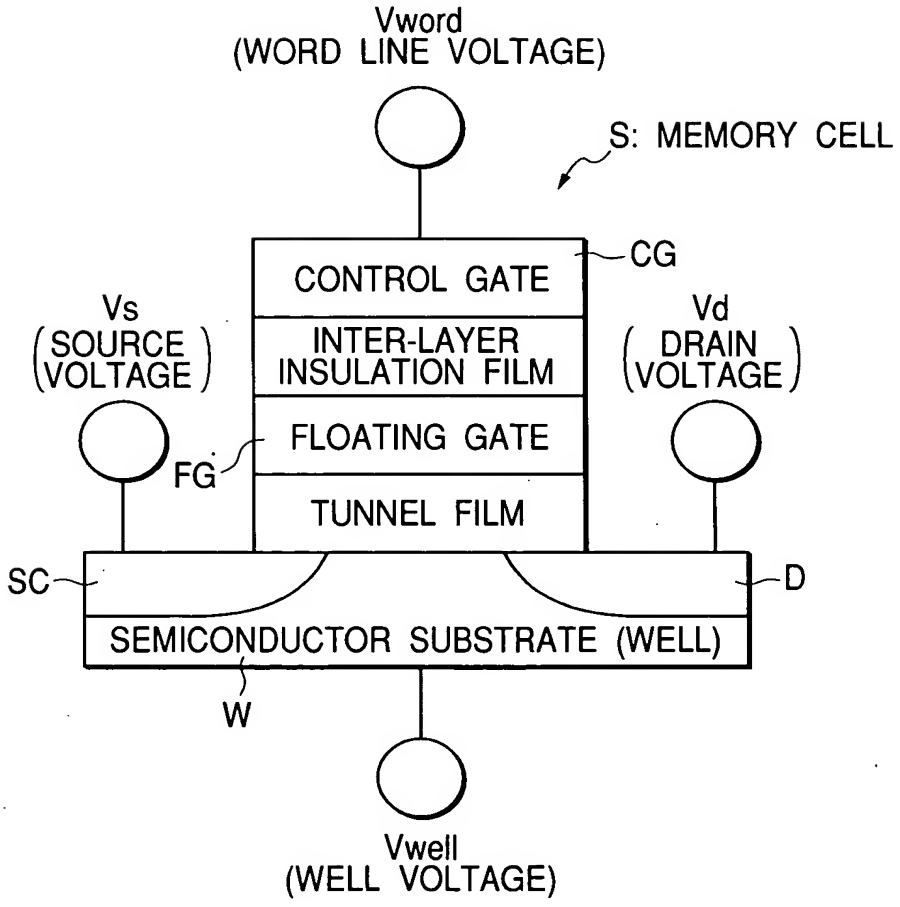

Vword
(WORD LINE VOLTAGE)
S: MEMORY CELL
CG
CONTROL GATE
INTER-LAYER
INSULATION FILM
FLOATING GATE
TUNNEL FILM
Vs
(SOURCE
VOLTAGE)
Vd
(DRAIN
VOLTAGE)
FG
SC
D
SEMICONDUCTOR SUBSTRATE (WELL)
W
Vwell
(WELL VOLTAGE)

FIG. 4(a)

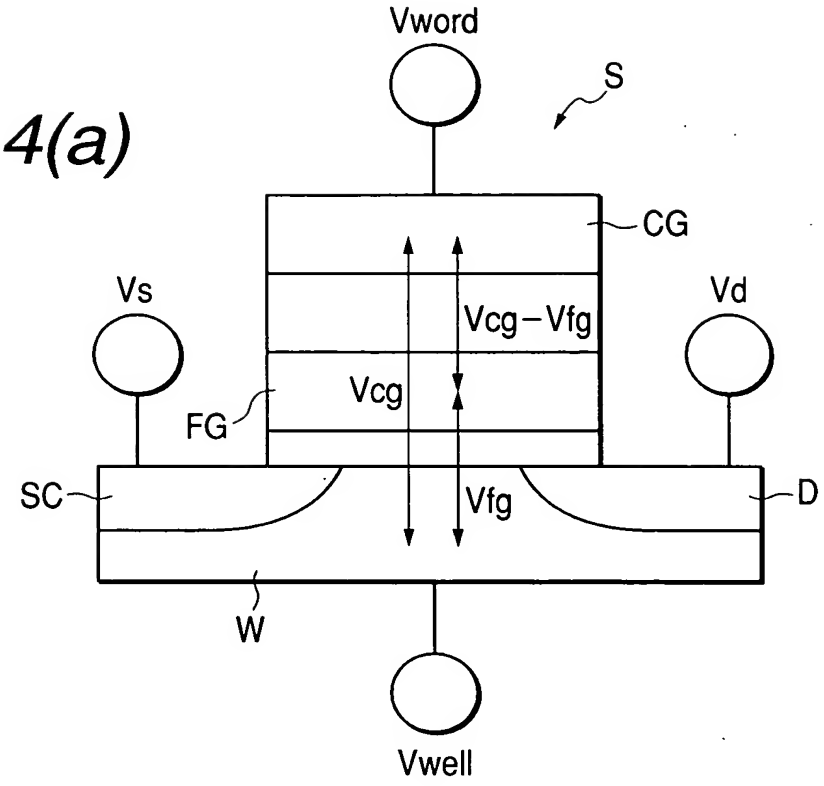
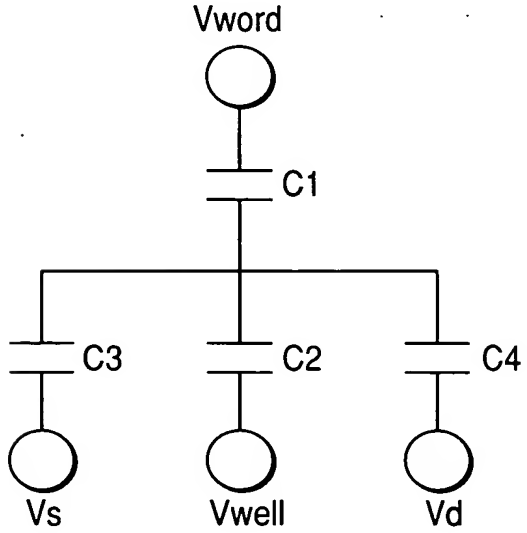


FIG. 4(b)



$Cr = C2/(C1+C2)$

$Cd = C3/(C1+C2)$ $Cs = C4/(C1+C2)$

$Vfg = Cr\cdot(Vcg-Vth+Vthi) + Cd\cdot Vd + Cs\cdot Vs$

NOTE) $Vcg = Vword-Vwell$

ELECTRICAL FIELD OF INTER-LAYER FILM = $Vcg-Vfg$

$Vthi = Vth$ IN THERMALLY EQUILIBRATED STATE

FIG. 5

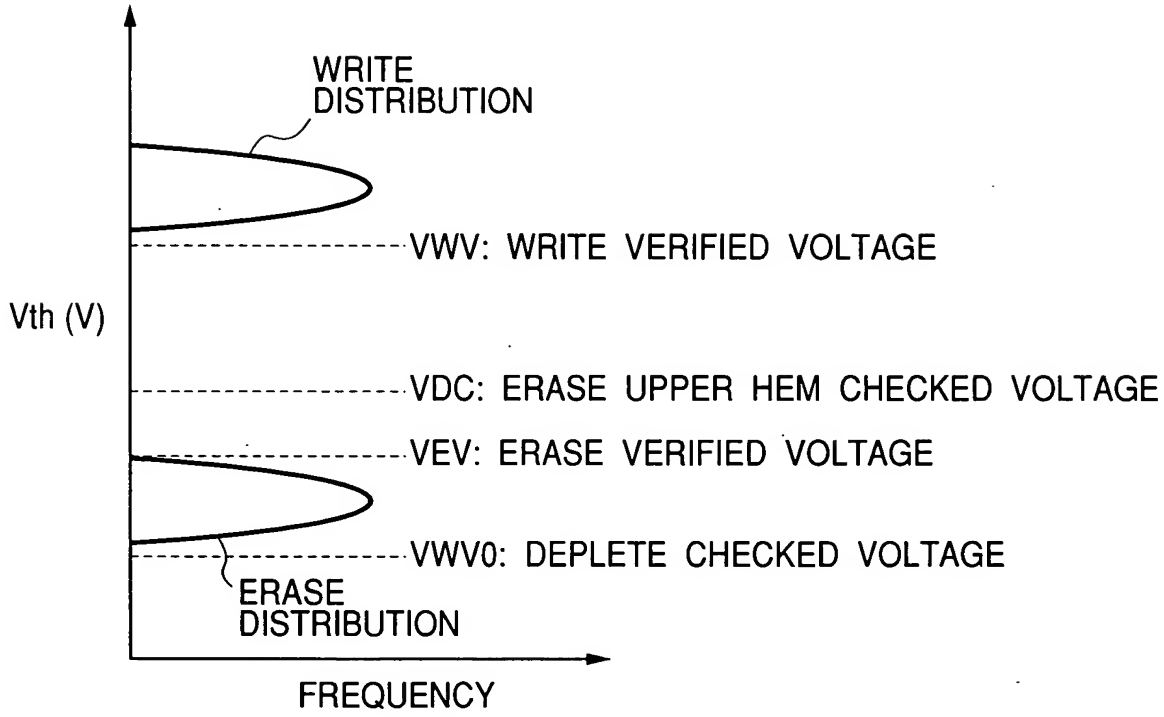

WRITE
DISTRIBUTION
VWV: WRITE VERIFIED VOLTAGE
Vth (V)
VDC: ERASE UPPER HEM CHECKED VOLTAGE
VEV: ERASE VERIFIED VOLTAGE
VWV0: DEPLETE CHECKED VOLTAGE
ERASE
DISTRIBUTION
FREQUENCY

FIG. 6

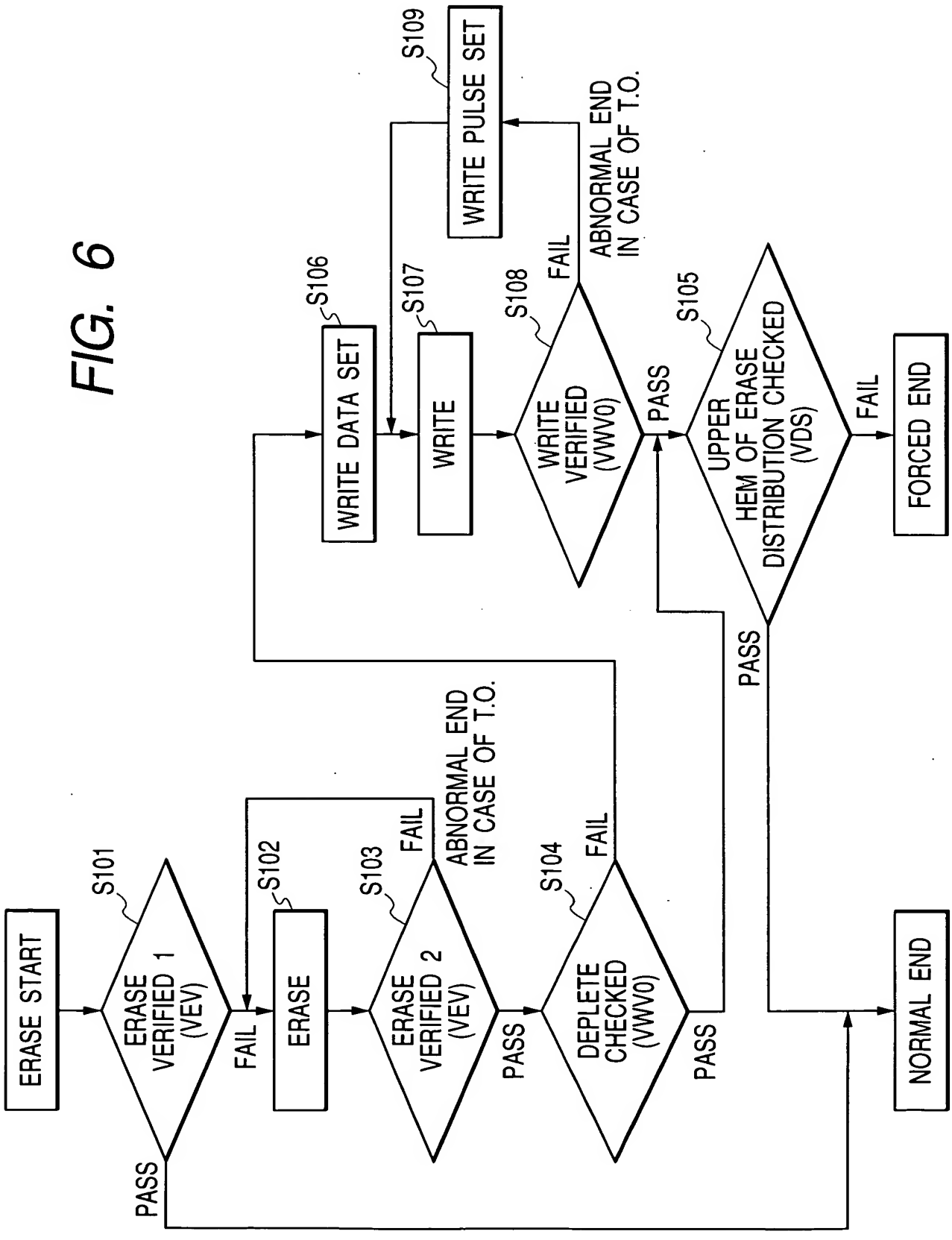

ERASE START
S101
ERASE VERIFIED 1 (VEV)
PASS
FAIL
S102
ERASE
S103
ERASE VERIFIED 2 (VEV)
FAIL
ABNORMAL END IN CASE OF T.O.
PASS
S104
DEPLETE CHECKED (VWV0)
FAIL
PASS
S105
UPPER HEM OF ERASE DISTRIBUTION CHECKED (VDS)
FAIL
FORCED END
PASS
NORMAL END
S106
WRITE DATA SET
S107
WRITE
S108
WRITE VERIFIED (VWV0)
FAIL
ABNORMAL END IN CASE OF T.O.
S109
WRITE PULSE SET

FIG. 7

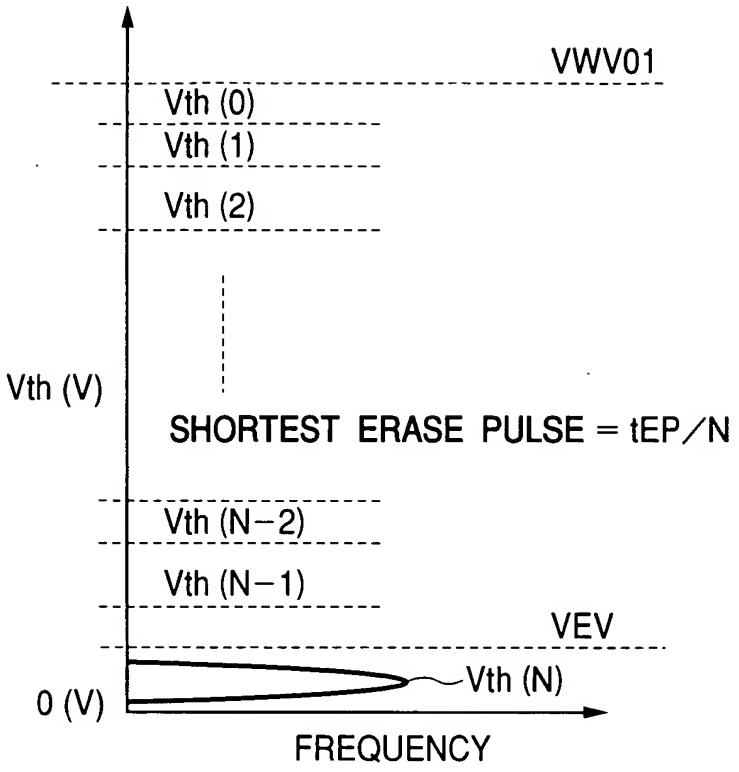

VWV01
Vth (0)
Vth (1)
Vth (2)
Vth (V)
SHORTEST ERASE PULSE = tEP/N
Vth (N−2)
Vth (N−1)
VEV
Vth (N)
0 (V)
FREQUENCY

FIG. 8

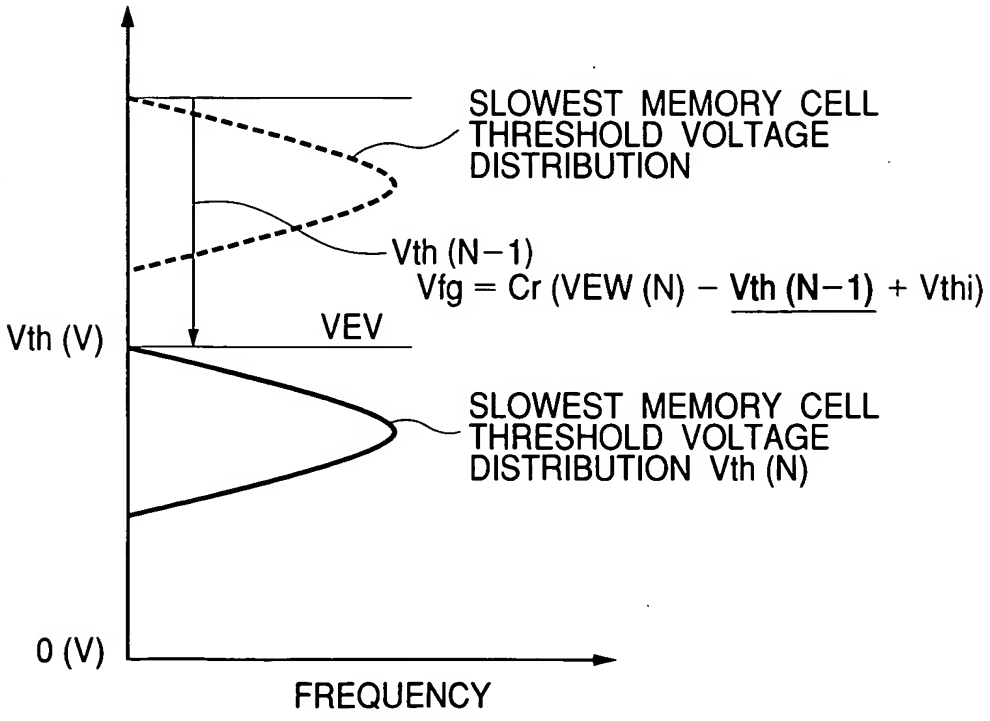

SLOWEST MEMORY CELL
THRESHOLD VOLTAGE
DISTRIBUTION
Vth (N−1)
Vfg = Cr (VEW (N) − Vth (N−1) + Vthi)
Vth (V)
VEV
SLOWEST MEMORY CELL
THRESHOLD VOLTAGE
DISTRIBUTION Vth (N)
0 (V)
FREQUENCY

FIG. 9

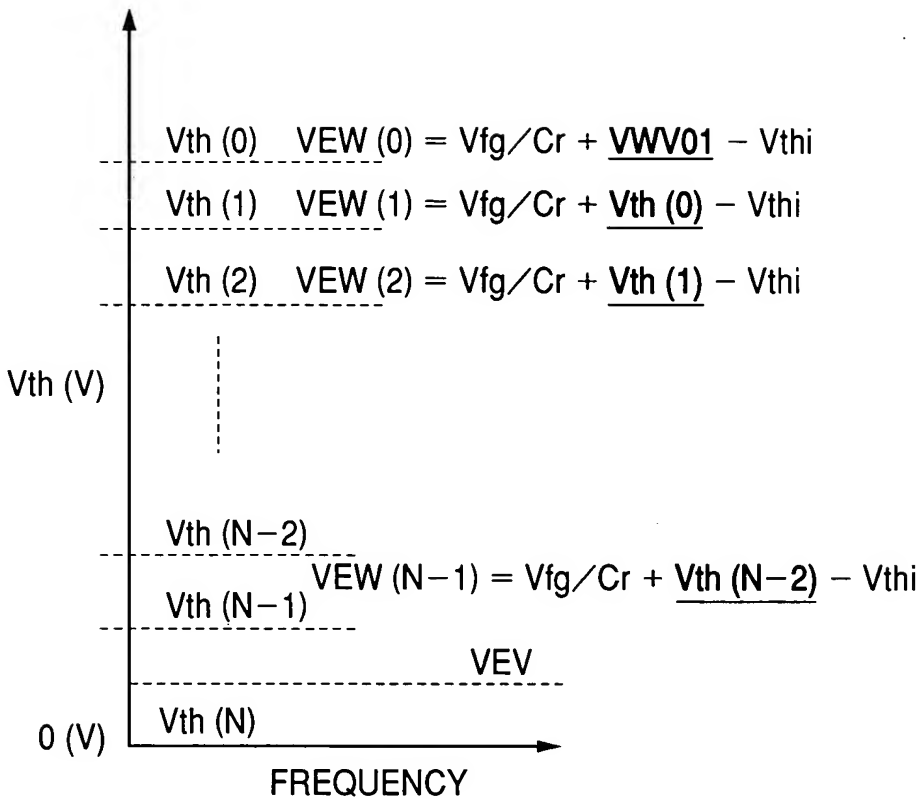

Vth (0) VEW (0) = Vfg/Cr + VWV01 − Vthi
Vth (1) VEW (1) = Vfg/Cr + Vth (0) − Vthi
Vth (2) VEW (2) = Vfg/Cr + Vth (1) − Vthi
Vth (V)
Vth (N−2)
VEW (N−1) = Vfg/Cr + Vth (N−2) − Vthi
Vth (N−1)
VEV
0 (V)
Vth (N)
FREQUENCY

FIG. 10

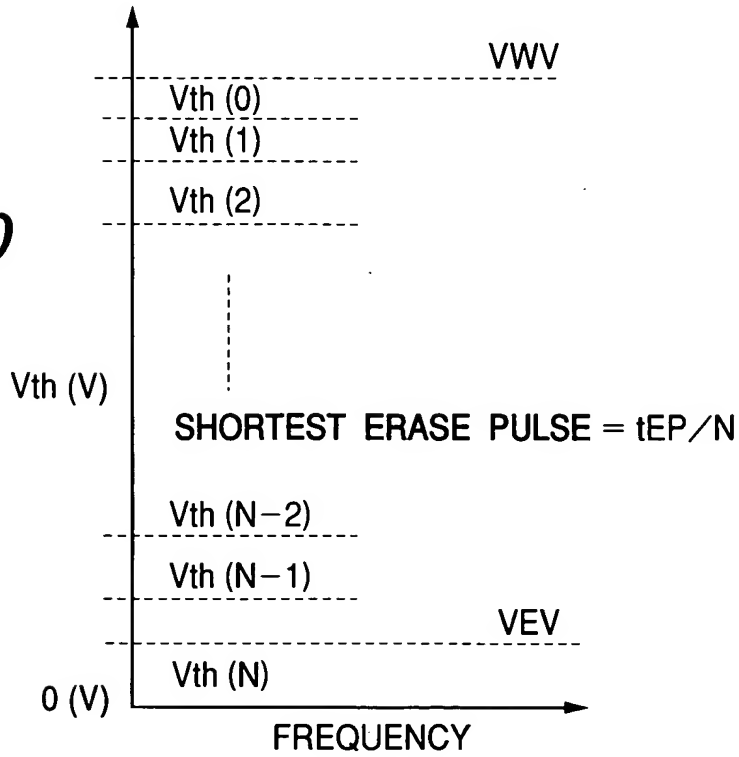

VWV
Vth (0)
Vth (1)
Vth (2)
Vth (V)
SHORTEST ERASE PULSE = tEP/N
Vth (N−2)
Vth (N−1)
VEV
0 (V)
Vth (N)
FREQUENCY

FIG. 11

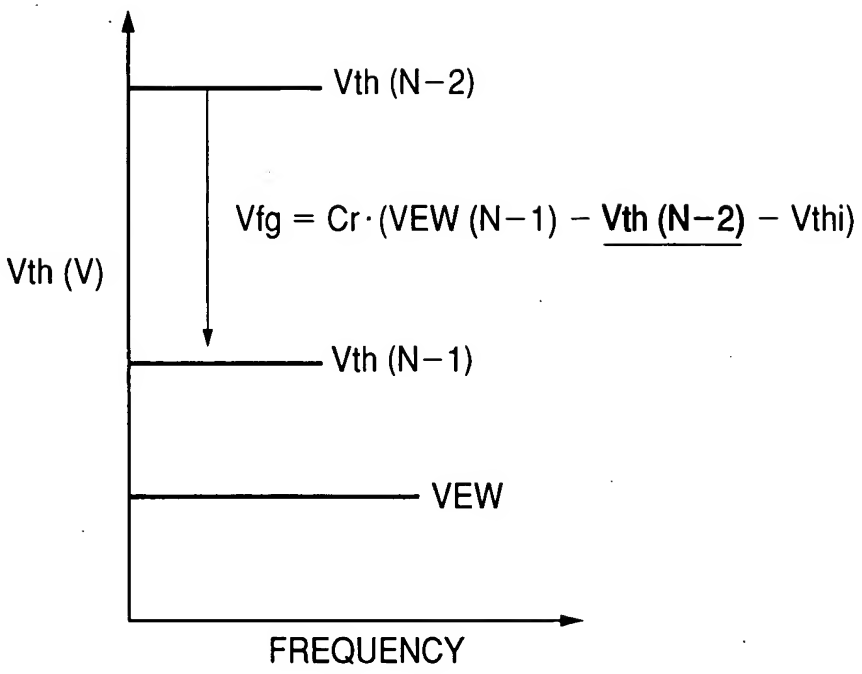

Vth (N−2)
Vfg = Cr·(VEW (N−1) − Vth (N−2) − Vthi)
Vth (V)
Vth (N−1)
VEW
FREQUENCY

FIG. 12

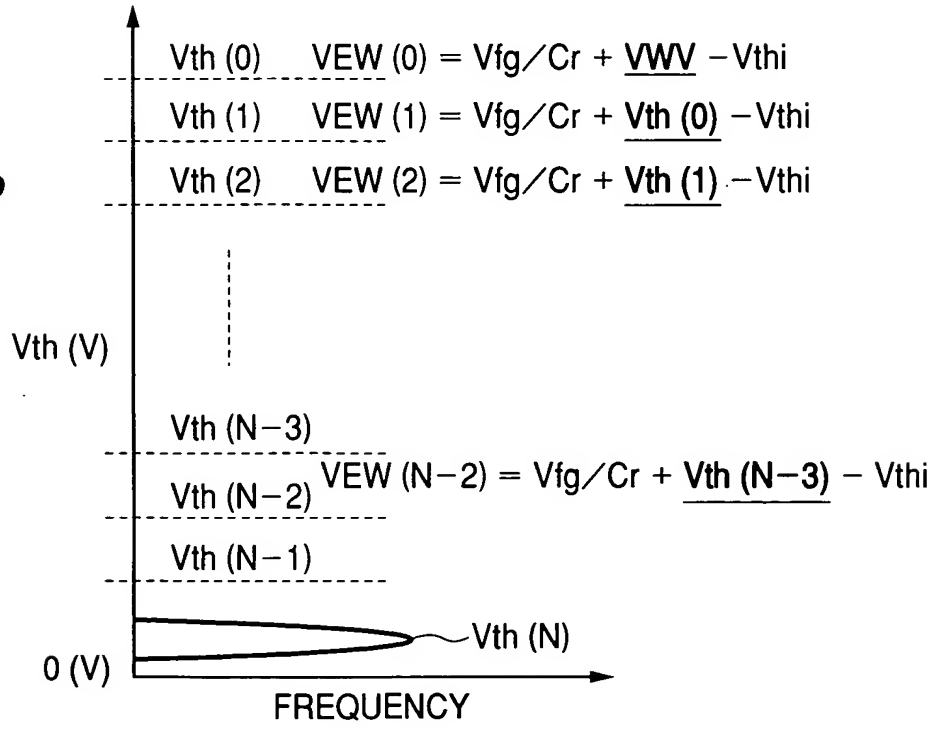

Vth (0) VEW (0) = Vfg/Cr + VWV −Vthi
Vth (1) VEW (1) = Vfg/Cr + Vth (0) −Vthi
Vth (2) VEW (2) = Vfg/Cr + Vth (1) −Vthi
Vth (V)
Vth (N−3)
VEW (N−2) = Vfg/Cr + Vth (N−3) − Vthi
Vth (N−2)
Vth (N−1)
Vth (N)
0 (V)
FREQUENCY

FIG. 13

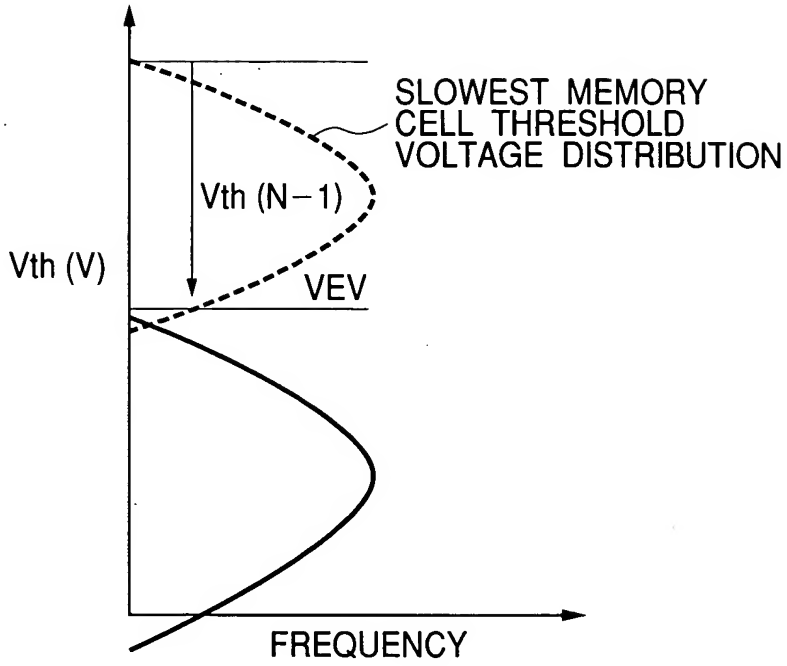

SLOWEST MEMORY
CELL THRESHOLD
VOLTAGE DISTRIBUTION
Vth (N−1)
Vth (V)
VEV
FREQUENCY

FIG. 14

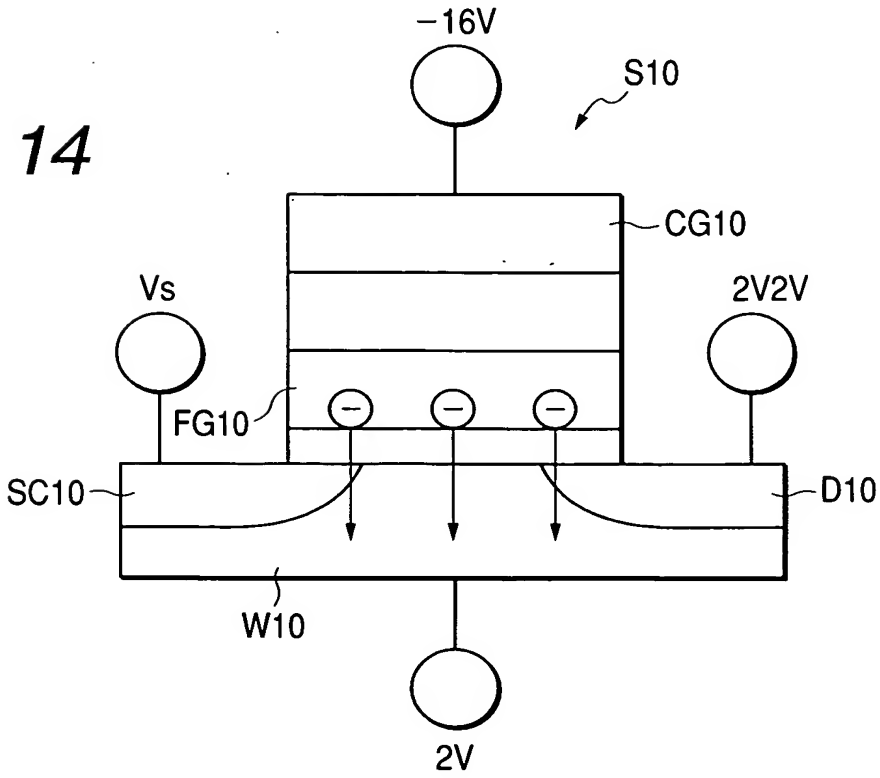

−16V
S10
CG10
Vs
2V2V
FG10
SC10
D10
W10
2V

FIG. 15

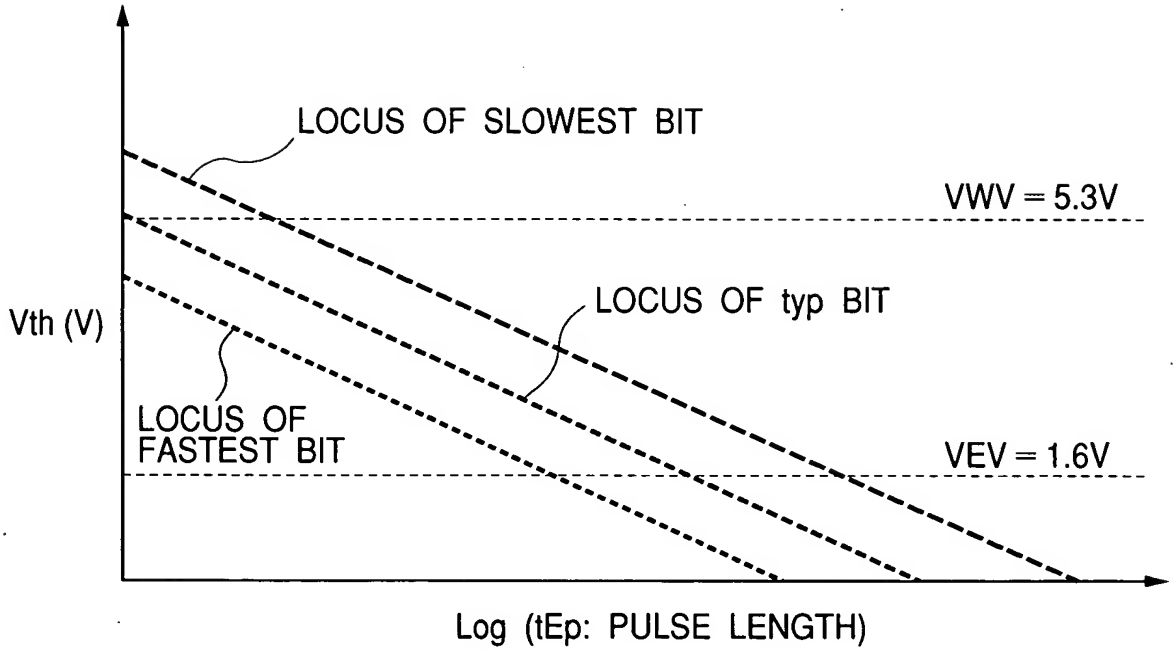

LOCUS OF SLOWEST BIT
VWV = 5.3V
LOCUS OF typ BIT
Vth (V)
LOCUS OF
FASTEST BIT
VEV = 1.6V
Log (tEp: PULSE LENGTH)

FIG. 16

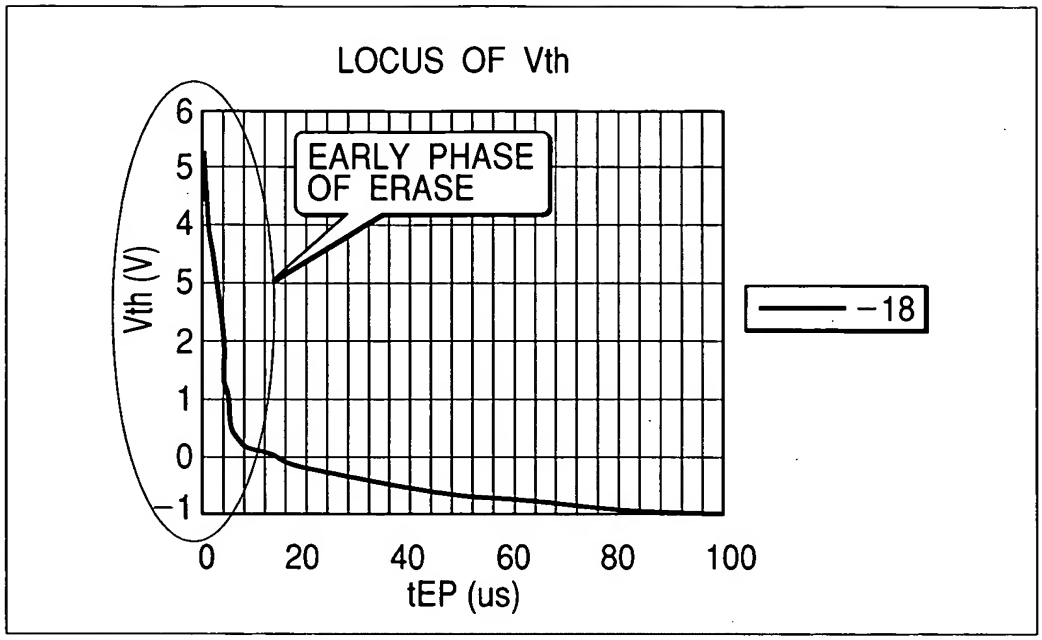

LOCUS OF Vth
EARLY PHASE OF ERASE
Vth (V)
6
5
4
5
2
1
0
−1
0
20
40
60
80
100
tEP (us)
−18

FIG. 17

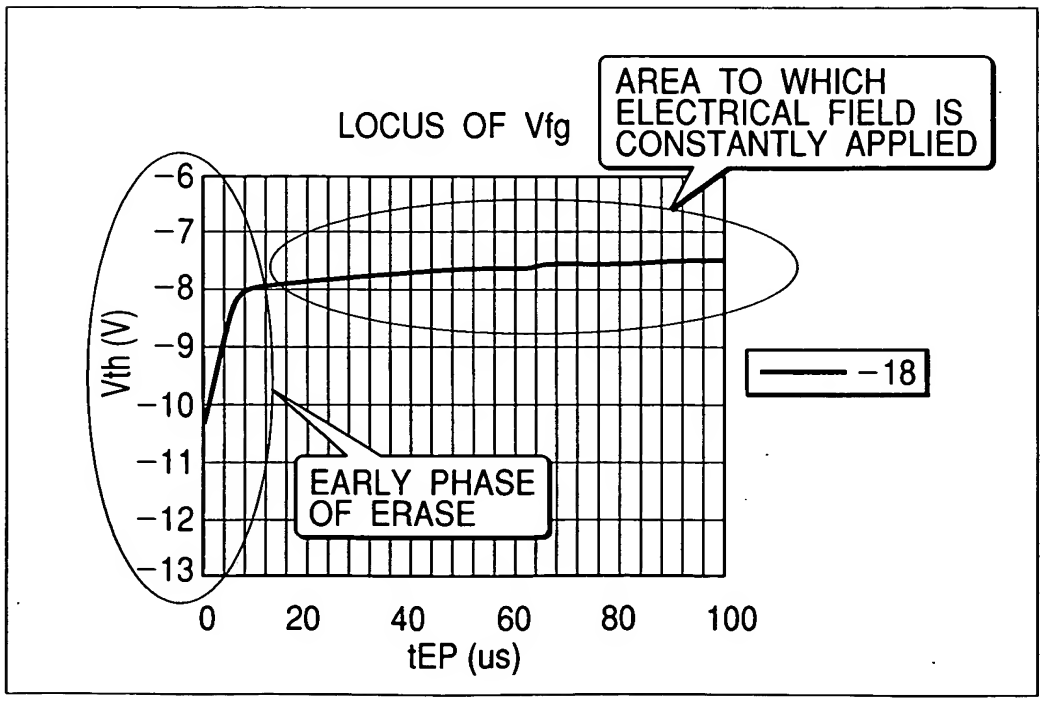

LOCUS OF Vfg
AREA TO WHICH ELECTRICAL FIELD IS CONSTANTLY APPLIED
EARLY PHASE OF ERASE
Vth (V)
−6
−7
−8
−9
−10
−11
−12
−13
0
20
40
60
80
100
tEP (us)
−18

FIG. 18

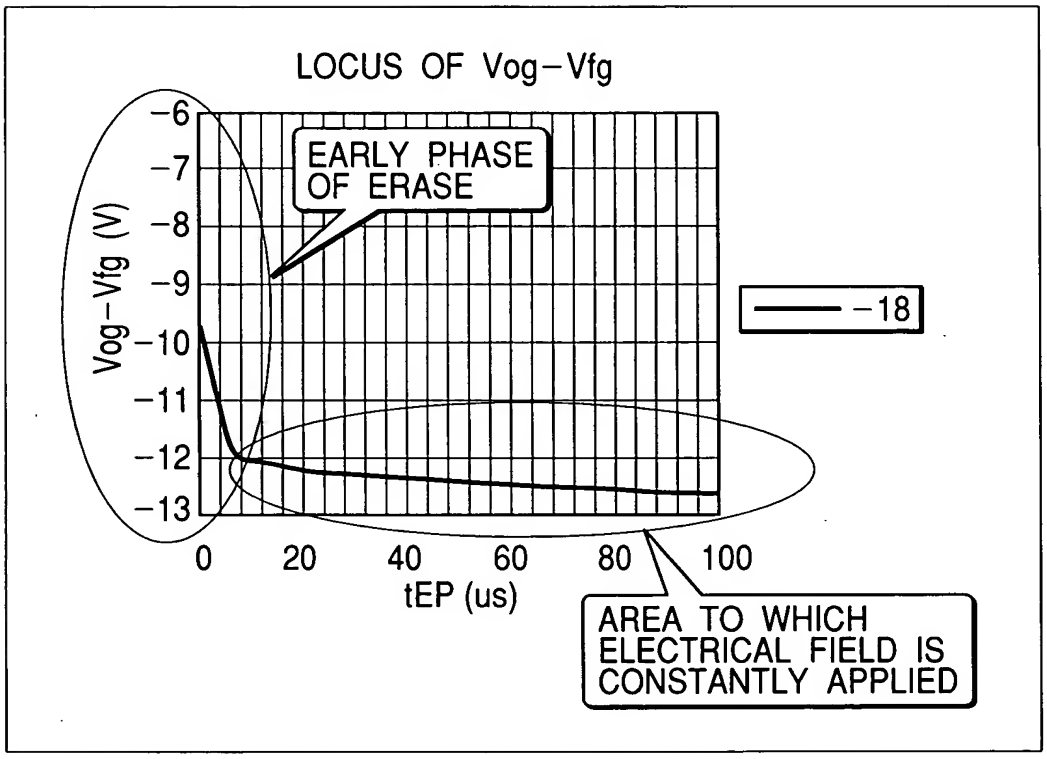

LOCUS OF Vog−Vfg
Vog−Vfg (V)
−6
−7
−8
−9
−10
−11
−12
−13
0
20
40
60
80
100
tEP (us)
EARLY PHASE OF ERASE
−18
AREA TO WHICH ELECTRICAL FIELD IS CONSTANTLY APPLIED

FIG. 19

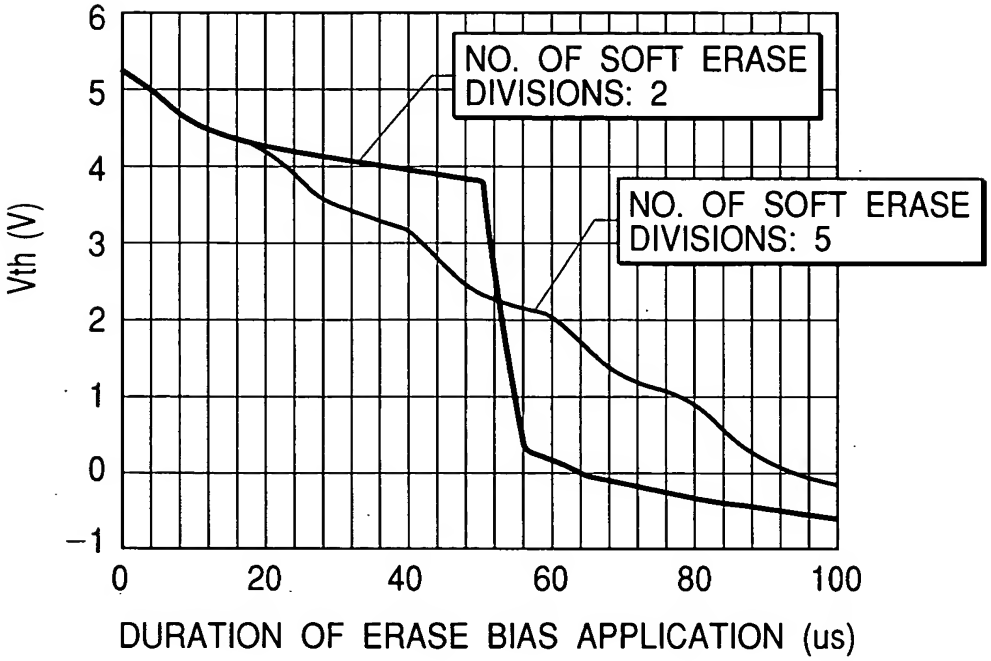

6
5
4
3
2
1
0
−1
Vth (V)
0
20
40
60
80
100
DURATION OF ERASE BIAS APPLICATION (us)
NO. OF SOFT ERASE DIVISIONS: 2
NO. OF SOFT ERASE DIVISIONS: 5

FIG. 20

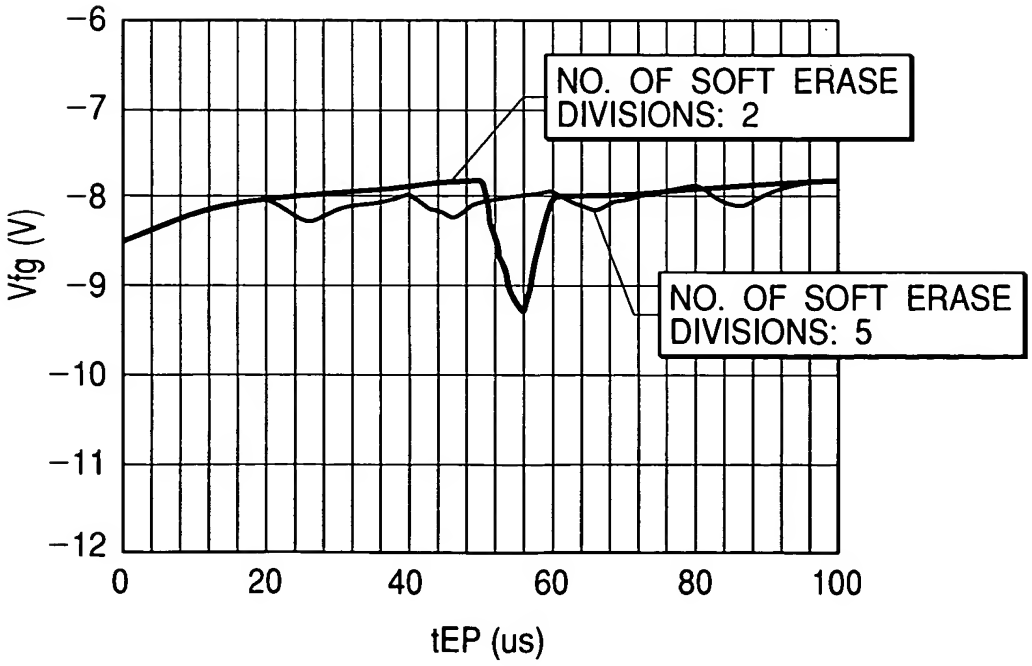
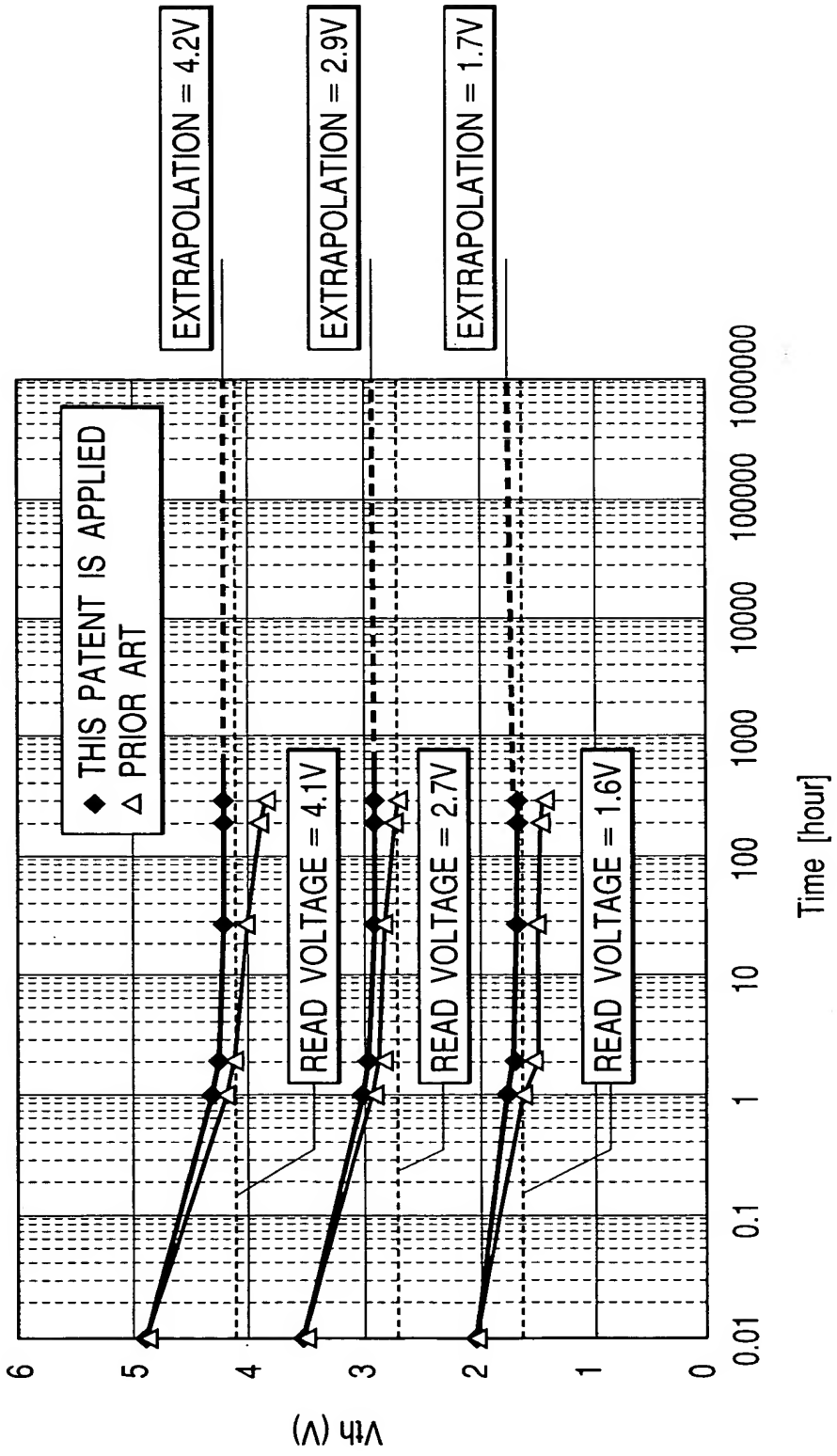

−6
−7
−8
−9
−10
−11
−12
Vfg (V)
0
20
40
60
80
100
tEP (us)
NO. OF SOFT ERASE DIVISIONS: 2
NO. OF SOFT ERASE DIVISIONS: 5

FIG. 21


◆ THIS PATENT IS APPLIED
△ PRIOR ART
EXTRAPOLATION = 4.2V
EXTRAPOLATION = 2.9V
EXTRAPOLATION = 1.7V
READ VOLTAGE = 4.1V
READ VOLTAGE = 2.7V
READ VOLTAGE = 1.6V
Vth (V)
Time [hour]
0
1
2
3
4
5
6
0.01
0.1
1
10
100
1000
10000
100000
1000000